Low-Voltage, Single and Dual Supply, 8 to 1 Multiplexer and Differential 4 to 1 Multiplexer

The Intersil ISL43681 and ISL43741 devices are precision, bidirectional, analog switches configured as an 8 channel and a differential 4 channel multiplexer/demultiplexer. They are designed to operate from a single +2V to +12V supply or from a ±2V to ±6V supplies. The devices have an inhibit and inhibit bar pin to simultaneously open all signal paths. The devices also have a latch bar pin to lock in the last switch address.

ON resistance of 39Ω with a ±5V supply and 125Ω with a +3.3V supply. Each switch can handle rail to rail analog signals. The off-leakage current is only 0.1nA at +25°C or 2.5nA at +85°C.

All digital inputs have 0.8V to 2.4V logic thresholds, ensuring TTL/CMOS logic compatibility when using a single 3.3V or +5V supply or dual ±5V supplies.

The ISL43681 is a single 8 to 1 multiplexer device and the ISL43741 is a diff 4 to 1 multiplexer device. Table 1 summarizes the performance of these parts.

TABLE 1. FEATURES AT A GLANCE

CONFIGURATION	SINGLE 8:1 MUX, DIFF 4:1 MUX
±5V R_{ON}	39Ω
±5V t_{ON}/t_{OFF}	32ns/18ns
12V R_{ON}	32Ω
12V t_{ON}/t_{OFF}	23ns/15ns
5V R_{ON}	65Ω
5V t_{ON}/t_{OFF}	38ns/19ns
3.3V R_{ON}	125Ω
3.3V t_{ON}/t_{OFF}	70ns/32ns
Package	20 Ld 4x4 QFN

Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- Application Note AN557 “Recommended Test Procedures for Analog Switches”
- Application Note AN520 “CMOS Analog Multiplexers and Switches; Specifications and Application Considerations.”
- Application Note AN1034 “Analog Switch and Multiplexer Applications”

Features

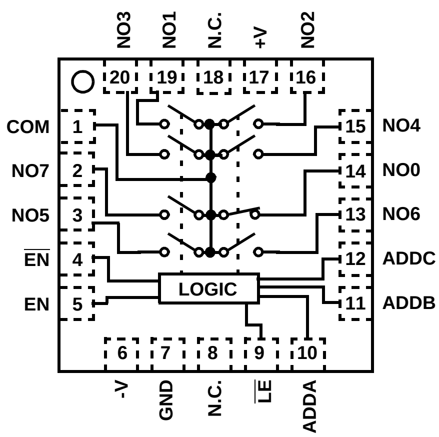
- Fully Specified at 3.3V, 5V, ±5V, and 12V Supplies for 10% Tolerances
- ON Resistance (R_{ON}) Max, V_S = ±4.5V. 50Ω
- ON Resistance (R_{ON}) Max, V_S = +3V 155Ω
- R_{ON} Matching Between Channels, V_S = ±5V. . . . .<2Ω
- Low Charge Injection, V_S = ±5V . . . . 1pC (Max)
- Single Supply Operation. . . . . +2V to +12V
- Dual Supply Operation . . . . ±2V to ±6V
- Fast Switching Action (V_S = +5V)
  - t_{ON} 38ns
  - t_{OFF} 19ns
- Guaranteed Max Off-leakage 2.5nA
- Guaranteed Break-Before-Make
- TTL, CMOS Compatible

Applications

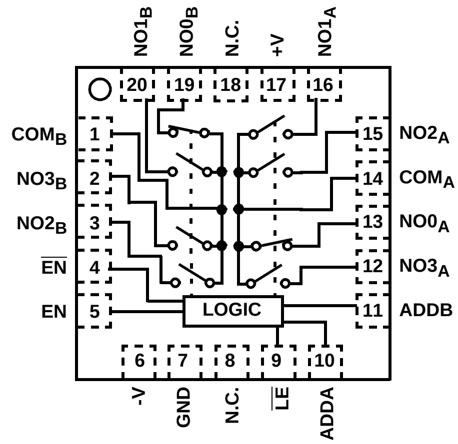
- Battery Powered, Handheld, and Portable Equipment
- Communications Systems
  - Radios
  - Telecom Infrastructure
  - ADSL, VDSL Modems
- Test Equipment
  - Medical Ultrasound
  - Magnetic Resonance Image
  - CT and PET Scanners (MRI)
  - ATE
  - Electrocardiograph
- Audio and Video Signal Routing
- Various Circuits
  - +3V/+5V DACs and ADCs
  - Sample and Hold Circuits
  - Operational Amplifier Gain Switching Networks
  - High Frequency Analog Switching
  - High Speed Multiplexing
  - Integrator Reset Circuits

Pinouts

ISL43681 (QFN)
TOP VIEW



ISL43741 (QFN)
TOP VIEW



Truth Tables

ISL43681

$\overline{LE}$	EN	$\overline{EN}$	ADDC	ADDB	ADDA	SWITCH ON
0	1	0	X	X	X	Last Switch Selected
X	0	X	X	X	X	NONE
X	X	1	X	X	X	NONE
1	1	0	0	0	0	NO0
1	1	0	0	0	1	NO1
1	1	0	0	1	0	NO2
1	1	0	0	1	1	NO3
1	1	0	1	0	0	NO4
1	1	0	1	0	1	NO5
1	1	0	1	1	0	NO6
1	1	0	1	1	1	NO7

NOTE: Logic "0" ≤0.8V. Logic "1" ≥2.4V, with V+ between 2.7V and 10V. X = Don't Care.

ISL43741

$\overline{LE}$	EN	$\overline{EN}$	ADDB	ADDA	SWITCH ON
0	1	0	X	X	Last Switch Selected
X	0	X	X	X	NONE
X	X	1	X	X	NONE
1	1	0	0	0	$NO0_A$, $NO0_B$
1	1	0	0	1	$NO1_A$, $NO1_B$
1	1	0	1	0	$NO2_A$, $NO2_B$
1	1	0	1	1	$NO3_A$, $NO3_B$

NOTE: Logic "0" ≤0.8V. Logic "1" ≥2.4V, with V+ between 2.7V and 10V. X = Don't Care.

Ordering Information

PART NO. (BRAND)	TEMP. RANGE (^oC)	PACKAGE	PKG. DWG. #
ISL43681IR (43681IR)	-40 to 85	20 Ld QFN	L20.4x4
ISL43741IR (43741IR)	-40 to 85	20 Ld QFN	L20.4x4

Pin Descriptions

PIN	FUNCTION
V+	Positive Power Supply Input
V-	Negative Power Supply Input. Connect to GND for Single Supply Configurations.
GND	Ground Connection
$\overline{EN}$	Digital Control Input. Connect to GND for Normal Operation. Connect to V+ to turn all switches off.
EN	Digital Control Input. Connect to V+ for Normal Operation. Connect to GND to turn all switches off.
$\overline{LE}$	Digital Control Input. Connect to +V for Normal Operation. Connect to GND to latch the last switch state.
COM	Analog Switch Common Pin
NO	Analog Switch Normally Open Pin
ADD	Address Input Pin
N.C.	No Internal Connection

Absolute Maximum Ratings

V+ to V- . . . . -0.3 to15V
V+ to GND . . . . -0.3 to15V
V- to GND . . . . -15 to 0.3V
Input Voltages
$\overline{LE}$, $\overline{EN}$, EN , NO, NC, ADD (Note 1) . . . . . . -0.3 to ((V+) + 0.3V)
Output Voltages
COM (Note 1). . . . . -0.3 to ((V+) + 0.3V)
Continuous Current (Any Terminal) . . . . ±30mA
Peak Current NO, NC, or COM
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . ±100mA
ESD Rating
HBM (Per Mil-STD-883, Method 3015.7) . . . . >2.5kV

Operating Conditions

Temperature Range
ISL43681IR and ISl43741IR . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} (°C/W)
20 Ld 4x4 QFN Package 45
Maximum Junction Temperature (Plastic Package) . . . . 150°C
Maximum Storage Temperature Range. . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Signals on NC, NO, COM, ADD, EN, $\overline{EN}$, or $\overline{LE}$ exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board with direct die attach. See Tech Brief TB379 for details.

Electrical Specifications ±5V Supply

Test Conditions: V_{SUPPLY} = ±4.5V to ±5.5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 3), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 4) MIN	TYP	(NOTE 4) MAX	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	V-	-	V+	V
ON Resistance, R_{ON}	V_S = ±4.5V, I_{COM} = 2mA, V_{NO} or V_{NC} = 3V (See Figure 6)	25	-	44	50	Ω
		Full	-	-	80	Ω
R_{ON} Matching Between Channels, ΔR_{ON}	V_S = ±4.5V, I_{COM} = 2mA, V_{NO} or V_{NC} = 3V (Note 5)	25	-	1.3	4	Ω
		Full	-	-	6	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V_S = ±4.5V, I_{COM} = 2mA, V_{NO} or V_{NC} = ±3V, 0V (Note 6)	25	-	7.5	9	Ω
		Full	-	-	12	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V_S = ±5.5V, V_{COM} = ±4.5V, V_{NO} or V_{NC} = ∓4.5V (Note 7)	25	-0.1	0.002	0.1	nA
		Full	-2.5	-	2.5	nA
COM OFF Leakage Current, $I_{COM(OFF)}$	V_S = ±5.5V, V_{COM} = ±4.5V, V_{NO} or V_{NC} = ∓4.5V (Note 7)	25	-0.1	0.002	0.1	nA
		Full	-2.5	-	2.5	nA
COM ON Leakage Current, $I_{COM(ON)}$	V_S = ±5.5V, V_{COM} = V_{NO} or V_{NC} = ±4.5V (Note 7)	25	-0.1	0.002	0.1	nA
		Full	-2.5	-	2.5	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}, V_{ADDH}		Full	2.4	-	-	V
Input Voltage Low, V_{INL}, V_{ADDL}		Full	-	-	0.8	V
Input Current, I_{ADDH}, I_{ADDL}, $I_{\overline{EN}H}$, $I_{\overline{EN}L}$	V_S = ±5.5V, V_{INH}, V_{ADD} = 0V or V+	Full	-0.5	-	0.5	µA
Input Current, I_{ENH}, $I_{\overline{LE}H}$	V_S = ±5.5V, V_{INH}, V_{ADD} = 0V or V+	Full	-1.5	-	1.5	µA
Input Current, I_{ENL}, $I_{\overline{LE}L}$	V_S = ±5.5V, V_{INH}, V_{ADD} = 0V or V+	Full	-4	-	4	µA

Electrical Specifications ±5V Supply

Test Conditions: V_{SUPPLY} = ±4.5V to ±5.5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 3), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS		TEMP (°C)	(NOTE 4) MIN	TYP	(NOTE 4) MAX	UNITS
DYNAMIC CHARACTERISTICS							
Enable Turn-ON Time, t_{ON}	V_S = ±4.5V, V_{NO} or V_{NC} = ±3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3 (See Figure 1)		25	-	35	50	ns
			Full	-	-	60	ns
Enable Turn-OFF Time, t_{OFF}	V_S = ±4.5V, V_{NO} or V_{NC} = ±3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3 (See Figure 1)		25	-	22	35	ns
			Full	-	-	40	ns
Address Transition Time, t_{TRANS}	V_S = ±4.5V, V_{NO} or V_{NC} = ±3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3 (See Figure 1)		25	-	43	60	ns
			Full	-	-	70	ns
Break-Before-Make Time, t_{BBM}	V_S = ±5.5V, V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (See Figure 3)		Full	2	7	-	ns
Latch Setup Time, t_S	(See Figure 4)		25	25	-	-	ns
			Full	35	-	-	ns
Latch Hold Time, t_H	(See Figure 4)		25	0	-	-	ns
			Full	0	-	-	ns
Latch Pulse Width, t_{WPW}	(See Figure 4)		25	15	-	-	ns
			Full	25	-		ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω (See Figure 2)		25	-	0.3	1	pC
NO/NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 8)		25	-	3	-	pF
COM OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 8)	ISL43681	25	-	21	-	pF
		ISL43741	25	-	12	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 8)	ISL43681	25	-	26	-	pF
		ISL43741	25	-	18	-	pF
OFF Isolation	R_L = 50Ω, C_L = 15pF, f = 100kHz, V_{NOx} = $1V_{RMS}$ (See Figures 5, 7 and 20)		25	-	92	-	dB
Crosstalk, (Note 8) (ISL43741 only)			25	-	<-110	-	dB
All Hostile Crosstalk, (Note 8) (ISL43741 only)			25	-	-105	-	dB
POWER SUPPLY CHARACTERISTICS							
Power Supply Range			Full	±2	-	±6	V
Positive Supply Current, I+	V_S = ±5.5V, V_{INH}, V_{ADD} = 0V or V+, Switch On or Off		Full	-7	-	7	µA
Negative Supply Current, I-			Full	-1	-	1	µA

NOTES:

3. V_{IN} = Input logic voltage to configure the device in a given state.
4. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
5. ΔR_{ON} = R_{ON} (MAX) - R_{ON} (MIN).
6. Flatness is defined as the difference between maximum and minimum value of on-resistance over the specified analog signal range.
7. Leakage parameter is 100% tested at high temp, and guaranteed by correlation at 25°C.
8. Between any two switches.

Electrical Specifications +12V Supply Test Conditions: V+ = +10.8V to +13.2V, GND = 0V, V_{INH} = 4V, V_{INL} = 0.8V (Note 3), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 4) MIN	TYP	(NOTE 4) MAX	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, R_{ON}	V+ = 10.8V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 9V (See Figure 6)	25	-	37	45	Ω
		Full	-	-	55	Ω
R_{ON} Matching Between Channels, ΔR_{ON}	V+ = 10.8V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 9V (Note 5)	25	-	1.2	2	Ω
		Full	-	-	2	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 10.8V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 3V, 6V, 9V (Note 6)	25	-	5	7	Ω
		Full	-	-	7	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 13.2V, V_{COM} = 1V, 12V, V_{NO} or V_{NC} = 12V, 1V (Note 7)	25	-0.1	0.002	0.1	nA
		Full	-2.5	-	2.5	nA
COM OFF Leakage Current, $I_{COM(OFF)}$	V+ = 13.2V, V_{COM} = 12V, 1V, V_{NO} or V_{NC} = 1V, 12V (Note 7)	25	-0.1	0.002	0.1	nA
		Full	-2.5	-	2.5	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 13.2V, V_{COM} = 1V, 12V, V_{NO} or V_{NC} = 1V, 12V, or floating (Note 7)	25	-0.1	0.002	0.1	nA
		Full	-2.5	-	2.5	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}, V_{ADDH}		Full	3.7	3.3	-	V
Input Voltage Low, V_{INL}, V_{ADDL}		Full	-	2.7	0.8	V
Input Current, I_{ADDH}, I_{ADDL}, $I_{\overline{EN}H}$, $I_{\overline{EN}L}$	V+ = 13.2V, V_{INH}, V_{ADD} = 0V or V+	Full	-0.5	-	0.5	µA
Input Current, I_{ENH}, $I_{\overline{LE}H}$	V+ = 13.2V, V_{INH}, V_{ADD} = 0V or V+	Full	-1.5	-	1.5	µA
Input Current, I_{ENL}, $I_{\overline{LE}L}$	V+ = 13.2V, V_{INH}, V_{ADD} = 0V or V+	Full	-4	-	4	µA
DYNAMIC CHARACTERISTICS						
Enable Turn-ON Time, t_{ON}	V+ = 10.8V, V_{NO} or V_{NC} = 10V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 4 (See Figure 1)	25	-	24	40	ns
		Full	-	-	45	ns
Enable Turn-OFF Time, t_{OFF}	V+ = 10.8V, V_{NO} or V_{NC} = 10V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 4 (See Figure 1)	25	-	15	30	ns
		Full	-	-	35	ns
Address Transition Time, t_{TRANS}	V+ = 10.8V, V_{NO} or V_{NC} = 10V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 4 (See Figure 1)	25	-	27	50	ns
		Full	-	-	55	ns
Break-Before-Make Time Delay, t_D	V+ = 13.2V, R_L = 300Ω, C_L = 35pF, V_{NO} or V_{NC} = 10V, V_{IN} = 0 to 4 (See Figure 3)	Full	2	5	-	ns
Latch Setup Time, t_S	(See Figure 4)	25	25	-	-	ns
		Full	35	-	-	ns
Latch Hold Time, t_H	(See Figure 4)	25	0	-	-	ns
		Full	0	-	-	ns
Latch Pulse Width, t_{WPW}	(See Figure 4)	25	15	-	-	ns
		Full	25	-	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω (See Figure 2)	25	-	2.7	5	pC

Electrical Specifications +12V Supply

Test Conditions: V+ = +10.8V to +13.2V, GND = 0V, V_{INH} = 4V, V_{INL} = 0.8V (Note 3), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS		TEMP (°C)	(NOTE 4) MIN	TYP	(NOTE 4) MAX	UNITS
OFF Isolation	R_L = 50Ω, C_L = 15pF, f = 100kHz (See Figure 5,7 and 20)		25	-	92	-	dB
Crosstalk, (Note 8), (ISL43741 only)			25	-	<-110	-	dB
All Hostile Crosstalk, (Note 8) (ISL43741 only)			25	-	-105	-	dB
NO or NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 8)		25	-	3	-	pF
COM OFF Capacitance, $C_{COM(OFF)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 8)	ISL43681	25	-	21	-	pF
		ISL43741	25	-	12	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 8)	ISL43681	25	-	26	-	pF
		ISL43741	25	-	18	-	pF
POWER SUPPLY CHARACTERISTICS							
Power Supply Range			Full	2	-	12	V
Positive Supply Current, I+	V+ = 13.2V, V_{INH}, V_{ADD} = 0V or V+, all channels on or off		Full	-7	-	7	µA
Positive Supply Current, I-			Full	-1	-	1	µA

Electrical Specifications 5V Supply

Test Conditions: V+ = +4.5V to +5.5V, V- = GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 3), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (NOTE 4)	TYP	MAX (NOTE 4)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, R_{ON}	V+ = 4.5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 3.5V (See Figure 6)	25	-	81	90	Ω
		Full	-	-	120	Ω
R_{ON} Matching Between Channels, ΔR_{ON}	V+ = 4.5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 3V (Note 5)	25	-	2.2	4	Ω
		Full	-	-	6	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 4.5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 1V, 2V, 3V (Note 6)	25	-	11.5	17	Ω
		Full	-	-	24	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 5.5V, V_{COM} = 1V, 4.5V, V_{NO} or V_{NC} = 4.5V, 1V (Note 7)	25	-0.1	0.002	0.1	nA
		Full	-2.5	-	2.5	nA
COM OFF Leakage Current, $I_{COM(OFF)}$	V+ = 5.5V, V_{COM} = 1V, 4.5V, V_{NO} or V_{NC} = 4.5V, 1V (Note 7)	25	-0.1	0.002	0.1	nA
		Full	-2.5	-	2.5	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 5.5V, V_{COM} = V_{NO} or V_{NC} = 4.5V (Note 7)	25	-0.1	0.002	0.1	nA
		Full	-2.5	-	2.5	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}, V_{ADDH}		Full	2.4	-	-	V
Input Voltage Low, V_{INL}, V_{ADDL}		Full	-	-	0.8	V
Input Current, I_{ADDH}, I_{ADDL}, $I_{\overline{EN}H}$, $I_{\overline{EN}L}$	V+ = 5.5V, V_{INH}, V_{ADD} = 0V or V+	Full	-0.5	-	0.5	µA
Input Current, I_{ENH}, $I_{\overline{LE}H}$	V+ = 5.5V, V_{INH}, V_{ADD} = 0V or V+	Full	-1.5	-	1.5	µA
Input Current, I_{ENL}, $I_{\overline{LE}L}$	V+ = 5.5V, V_{INH}, V_{ADD} = 0V or V+	Full	-4	-	4	µA

Electrical Specifications 5V Supply

Test Conditions: V+ = +4.5V to +5.5V, V- = GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 3), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (NOTE 4)	TYP	MAX (NOTE 4)	UNITS
DYNAMIC CHARACTERISTICS						
Enable Turn-ON Time, t_{ON}	V+ = 4.5V, V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (See Figure 1)	25	-	43	60	ns
		Full	-	-	70	ns
Enable Turn-OFF Time, t_{OFF}	V+ = 4.5V, V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (See Figure 1)	25	-	20	35	ns
		Full	-	-	40	ns
Address Transition Time, t_{TRANS}	V+ = 4.5V, V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (See Figure 1)	25	-	51	70	ns
		Full	-	-	85	ns
Break-Before-Make Time, t_{BBM}	V+ = 5.5V, V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (See Figure 3)	Full	2	9	-	ns
Latch Setup Time, t_S	(See Figure 4)	25	25	-	-	ns
		Full	35	-	-	ns
Latch Hold Time, t_H	(See Figure 4)	25	0	-	-	ns
		Full	0	-	-	ns
Latch Pulse Width, t_{WPW}	(See Figure 4)	25	15	-	-	ns
		Full	25	-	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω (See Figure 2)	25	-	0.6	1.5	pC
OFF Isolation	R_L = 50Ω, C_L = 15pF, f = 100kHz, V_{NOx} = 1V_{RMS} (See Figures 5, 7 and 20)	25	-	92	-	dB
Crosstalk, (Note 8), (ISL43741 only)		25	-	<-110	-	dB
All Hostile Crosstalk, (Note 8), (ISL43741 only)		25	-	-105	1.5	dB
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	2	-	12	V
Positive Supply Current, I+	V+ = 5.5V, V- = 0V, V_{INH}, V_{ADD} = 0V or V+, Switch On or Off	Full	-7	-	7	µA
Positive Supply Current, I-		Full	-1	-	1	µA

Electrical Specifications 3.3V Supply

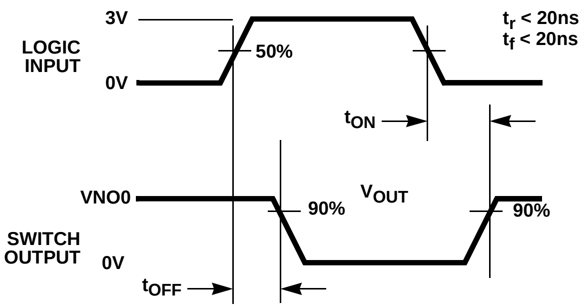
Test Conditions: V+ = +3.0V to +3.6V, V- = GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 3), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (NOTE 4)	TYP	MAX (NOTE 4)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, R_{ON}	V+ = 3.0V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 1.5V (See Figure 6)	25	-	135	155	Ω
		Full	-	-	200	Ω
R_{ON} Matching Between Channels, ΔR_{ON}	V+ = 3.0V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 1.5V (Note 5)	25	-	3.4	8	Ω
		Full	-	-	10	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 3.0V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 0.5V, 1V, 2V (Note 6)	25	-	34	40	Ω
		Full	-	-	50	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 3.6V, V_{COM} = 0V, 4.5V, V_{NO} or V_{NC} = 3V, 1V (Note 7)	25	-0.1	0.002	0.1	nA
		Full	-2.5	-	2.5	nA

Electrical Specifications 3.3V Supply Test Conditions: V+ = +3.0V to +3.6V, V- = GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 3), Unless Otherwise Specified **(Continued)**

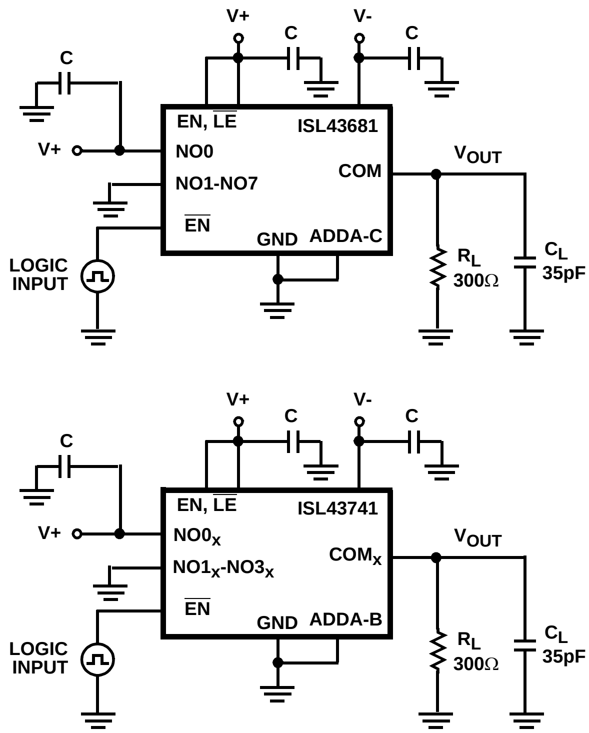
PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (NOTE 4)	TYP	MAX (NOTE 4)	UNITS
COM OFF Leakage Current, $I_{COM(OFF)}$	V+ = 3.6V, V_{COM} = 0V, 4.5V, V_{NO} or V_{NC} = 3V, 1V (Note 7)	25	-0.1	0.002	0.1	nA
		Full	-2.5	-	2.5	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 3.6V, V_{COM} = V_{NO} or V_{NC} = 3V (Note 7)	25	-0.1	0.002	0.1	nA
		Full	-2.5	-	2.5	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}, V_{ADDH}		Full	2.4	-	-	V
Input Voltage Low, V_{INL}, V_{ADDL}		Full	-	-	0.8	V
Input Current, I_{ADDH}, I_{ADDL}, $I_{\overline{EN}H}$, $I_{\overline{EN}L}$	V+ = 3.6V, V_{INH}, V_{ADD} = 0V or V+	Full	-0.5	-	0.5	µA
Input Current, I_{ENH}, $I_{\overline{LE}H}$	V+ = 3.6V, V_{INH}, V_{ADD} = 0V or V+	Full	-1.5	-	1.5	µA
Input Current, I_{ENL}, $I_{\overline{LE}L}$	V+ = 3.6V, V_{INH}, V_{ADD} = 0V or V+	Full	-4	-	4	µA
DYNAMIC CHARACTERISTICS						
Enable Turn-ON Time, t_{ON}	V+ = 3.0V, V_{NO} or V_{NC} = 1.5V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (See Figure 1)	25	-	82	100	ns
		Full	-	-	120	ns
Enable Turn-OFF Time, t_{OFF}	V+ = 3.0V, V_{NO} or V_{NC} = 1.5V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (See Figure 1)	25	-	37	50	ns
		Full	-	-	60	ns
Address Transition Time, t_{TRANS}	V+ = 3.0V, V_{NO} or V_{NC} = 1.5V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (See Figure 1)	25	-	96	120	ns
		Full	-	-	145	ns
Break-Before-Make Time, t_{BBM}	V+ = 3.6V, V_{NO} or V_{NC} = 1.5V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (See Figure 3)	Full	3	13	-	ns
Latch Setup Time, t_S	(See Figure 4)	25	50	-	-	ns
		Full	60	-	-	ns
Latch Hold Time, t_H	(See Figure 4)	25	0	-	-	ns
		Full	0	-	-	ns
Latch Pulse Width, t_{WPW}	(See Figure 4)	25	30	-	-	ns
		Full	40	-	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω (See Figure 2)	25	-	0.3	1	pC
OFF Isolation	R_L = 50Ω, C_L = 15pF, f = 100kHz, V_{NO} or V_{NC} = $1V_{RMS}$ (See Figures 5, 7 and 20)	25	-	92	-	dB
Crosstalk, (Note 8), (ISL43741 only)		25	-	<-110	-	dB
All Hostile Crosstalk, (Note 8), (ISL43741 only)		25	-	-105	-	dB
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	2	-	12	V
Positive Supply Current, I+	V+ = 3.6V, V- = 0V, V_{INH}, V_{ADD} = 0V or V+, Switch On or Off	Full	-7	-	7	µA
Positive Supply Current, I-		Full	-1	-	1	µA

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. ENABLE t_{ON}/t_{OFF} MEASUREMENT POINTS

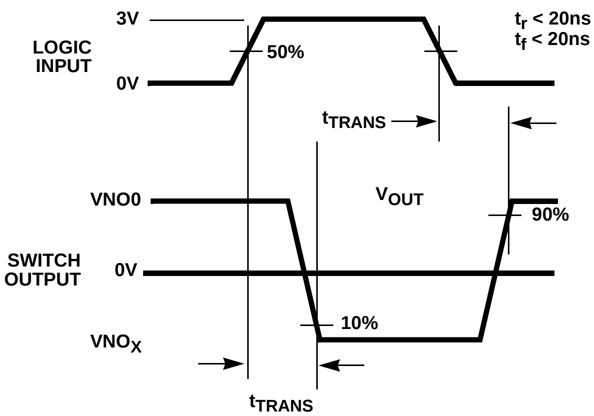


Repeat test for other switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + R_{(ON)}}$$

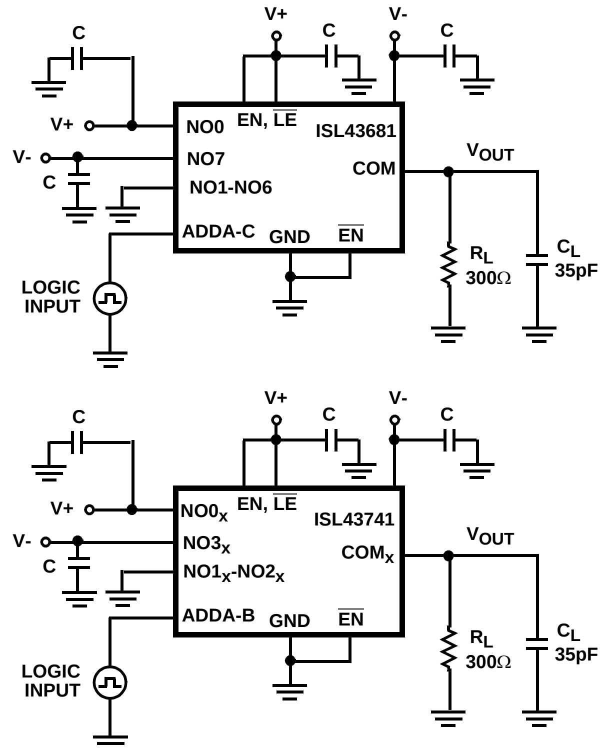
FIGURE 1B. ENABLE t_{ON}/t_{OFF} TEST CIRCUIT

Test Circuits and Waveforms (Continued)



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1C. ADDRESS t_{TRANS} MEASUREMENT POINTS



Repeat test for other switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + R_{(ON)}}$$

FIGURE 1D. ADDRESS t_{TRANS} TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

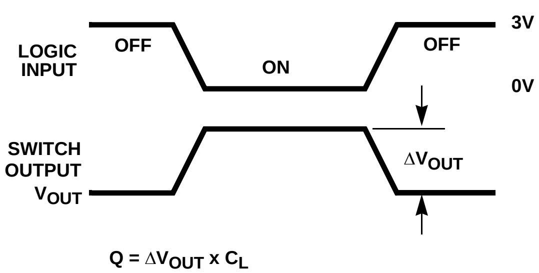
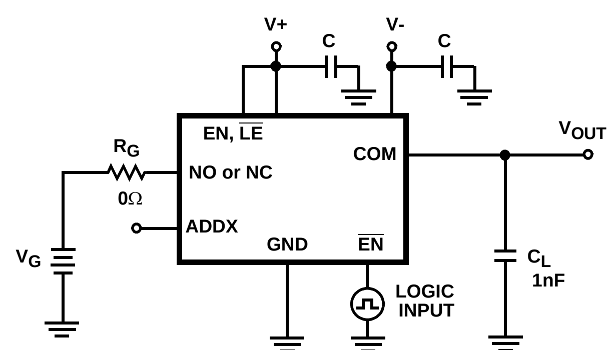


FIGURE 2A. Q MEASUREMENT POINTS



Repeat test for other switches.

FIGURE 2B. Q TEST CIRCUIT

FIGURE 2. CHARGE INJECTION

Test Circuits and Waveforms (Continued)

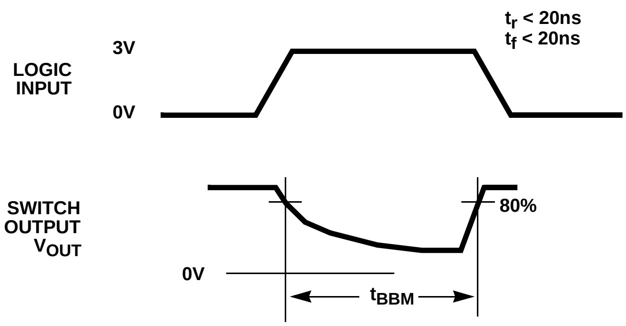
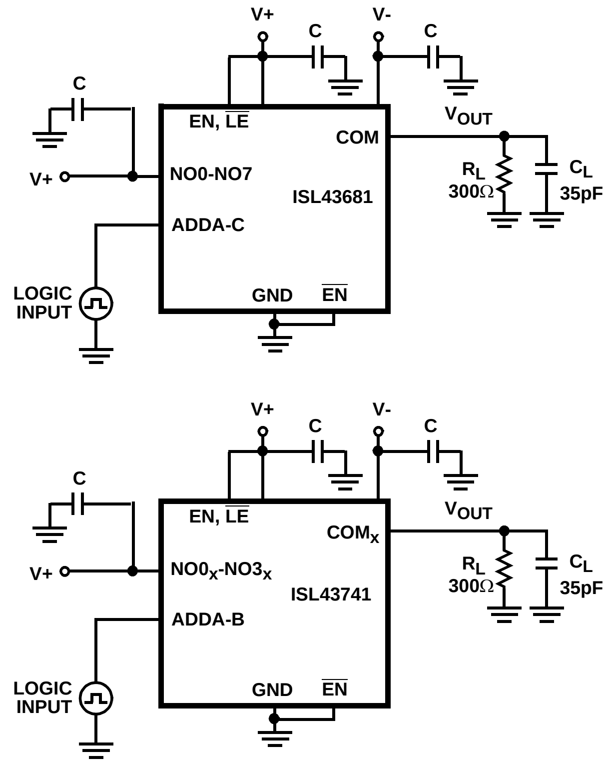


FIGURE 3A. t_{BBM} MEASUREMENT POINTS

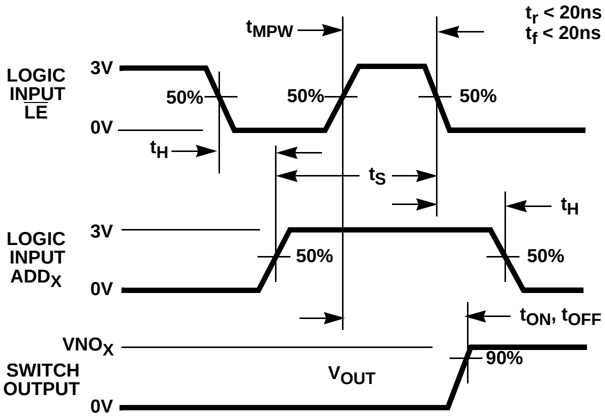


Repeat test for other switches. C_L includes fixture and stray capacitance.

FIGURE 3B. t_{BBM} TEST CIRCUIT

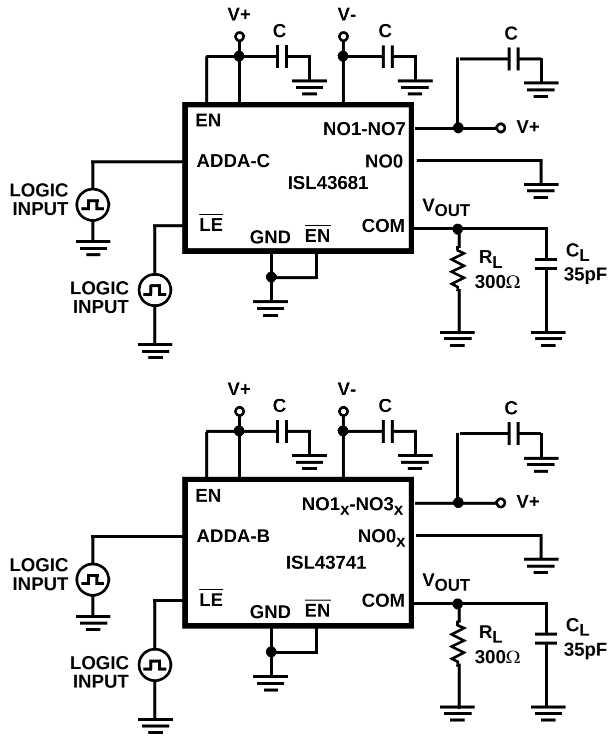
FIGURE 3. BREAK-BEFORE-MAKE TIME

Test Circuits and Waveforms (Continued)



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 4A. LATCH t_S, t_H, t_{MPW} MEASUREMENT POINTS



Repeat test for other switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + R_{(ON)}}$$

FIGURE 4B. LATCH t_S, t_H, t_{MPW} TEST CIRCUIT

FIGURE 4. LATCH SETUP AND HOLD TIMES

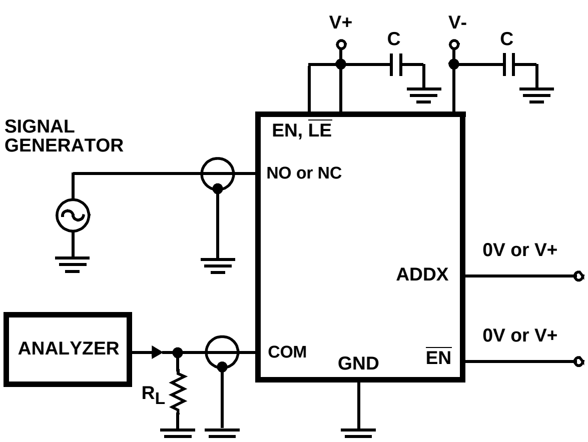


FIGURE 5. OFF ISOLATION TEST CIRCUIT

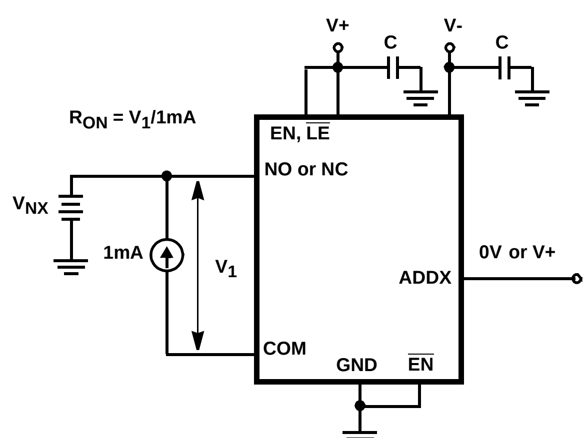


FIGURE 6. R_{ON} TEST CIRCUIT

Test Circuits and Waveforms (Continued)

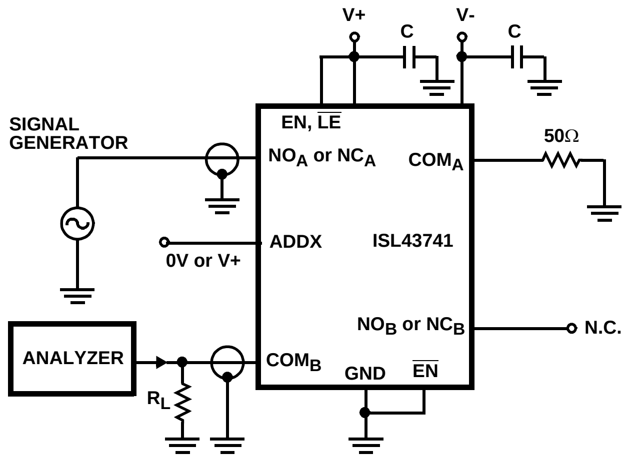


FIGURE 7. CROSSTALK TEST CIRCUIT

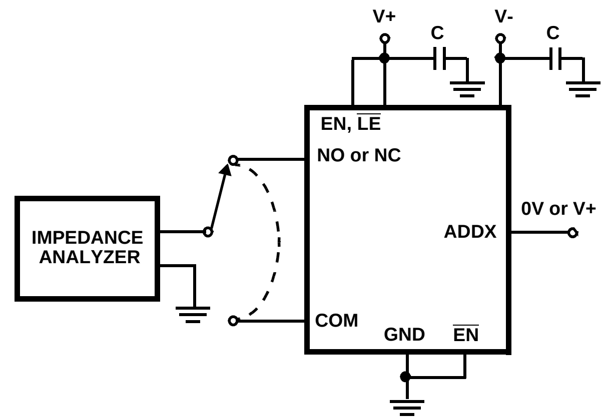


FIGURE 8. CAPACITANCE TEST CIRCUIT

Detailed Description

The ISL43681 and ISL43741 multiplexers offer precise switching capability from a bipolar ±2V to ±6V or a single 2V to 12V supply with low on-resistance (39Ω) and high speed operation (t_{ON} = 38ns, t_{OFF} = 19ns) with dual 5V supplies.

They have an inhibit and inhibit bar pin to simultaneously open all signal paths. They also have a latch bar pin to lock in the last switch address.

The devices are especially well suited for applications using ±5V supplies. With ±5V supplies the performance (R_{ON}, Leakage, Charge Injection, etc.) is best in class.

High frequency applications also benefit from the wide bandwidth, and the very high off isolation and crosstalk rejection.

Supply Sequencing And Overvoltage Protection

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents which might permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to V+ and to V- (see Figure 9). To prevent forward biasing these diodes, V+ and V- must be applied before any input signals, and input signal voltages must remain between V+ and V-. If these conditions cannot be guaranteed, then one of the following two protection methods should be employed.

Logic inputs can easily be protected by adding a 1kΩ resistor in series with the input (see Figure 9). The resistor limits the input current below the threshold that produces permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

This method is not applicable for the signal path inputs. Adding a series resistor to the switch input defeats the purpose of using a low R_{ON} switch, so two small signal diodes can be added in series with the supply pins to provide overvoltage protection for all pins (see Figure 9). These additional diodes limit the analog signal from 1V below V+ to 1V above V-. The low leakage current performance is unaffected by this approach, but the switch resistance may increase, especially at low supply voltages.

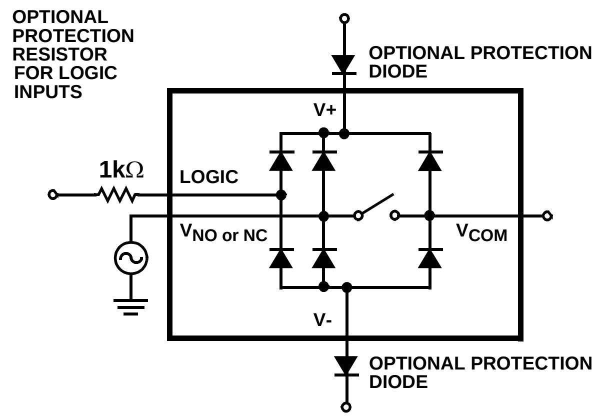


FIGURE 9. INPUT OVERVOLTAGE PROTECTION

Power-Supply Considerations

The ISL43681 and ISL43741 construction is typical of most CMOS analog switches, in that they have three supply pins: V+, V-, and GND. V+ and V- drive the internal CMOS switches and set their analog voltage limits, so there are no connections between the analog signal path and GND. Unlike switches with a 13V maximum supply voltage, the ISL43681 and ISL43741 15V maximum supply voltage provides plenty of room for the 10% tolerance of 12V supplies (±6V or 12V single supply), as well as room for overshoot and noise spikes.

This family of switches performs equally well when operated with bipolar or single voltage supplies.The minimum

recommended supply voltage is 2V or ±2V. It is important to note that the input signal range, switching times, and on-resistance degrade at lower supply voltages. Refer to the electrical specification tables and *Typical Performance* curves for details.

V+ and GND power the internal logic (thus setting the digital switching point) and level shifters. The level shifters convert the logic levels to switched V+ and V- signals to drive the analog switch gate terminals.

Logic-Level Thresholds

V+ and GND power the internal logic stages, so V- has no affect on logic thresholds. This switch family is TTL compatible (0.8V and 2.4V) over a V+ supply range of 2.7V to 10V. At 12V the V_{IH} level is about 3.3V. This is still below the CMOS guaranteed high output minimum level of 4V, but noise margin is reduced. For best results with a 12V supply, use a logic family that provides a V_{OH} greater than 4V.

The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails. Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat even past 100MHz (see Figures 18 and 19). Figures 18 and 19 also illustrates that the frequency response is very consistent over varying analog signal levels.

An OFF switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feed through from a switch's input to its output. Off Isolation is the resistance to this feed through, while Crosstalk indicates the amount of feed through from one switch to another. Figure 20 details the high Off Isolation and Crosstalk rejection provided by this family. At 10MHz, Off Isolation is about 55dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease Off Isolation and Crosstalk rejection due to the voltage divider action of the switch OFF impedance and the load impedance.

Leakage Considerations

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and V-. One of these diodes conducts if any analog signal exceeds V+ or V-.

Virtually all the analog leakage current comes from the ESD diodes to V+ or V-. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and V- pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog signal paths and GND.

Typical Performance Curves $T_A = 25^oC$, Unless Otherwise Specified

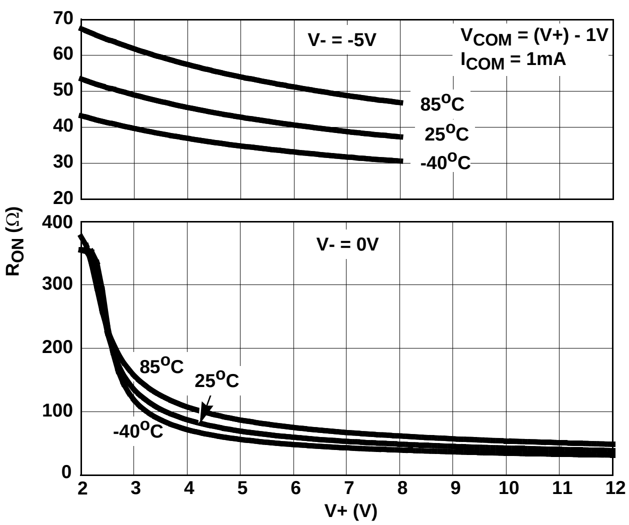


FIGURE 10. ON RESISTANCE vs SUPPLY VOLTAGE

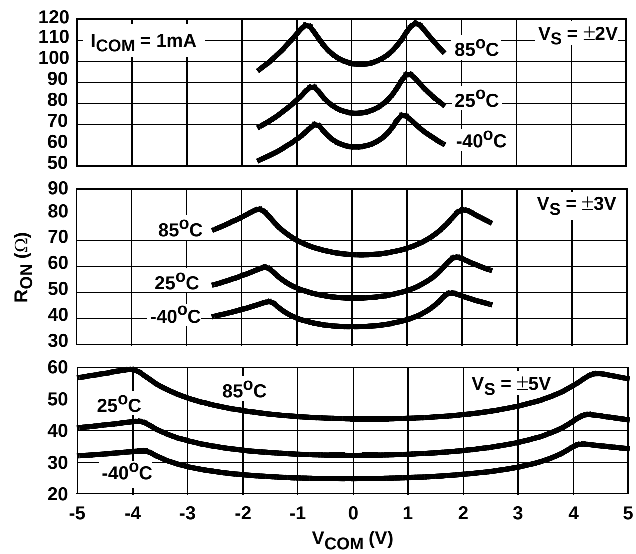


FIGURE 11. ON RESISTANCE vs SWITCH VOLTAGE

Typical Performance Curves $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

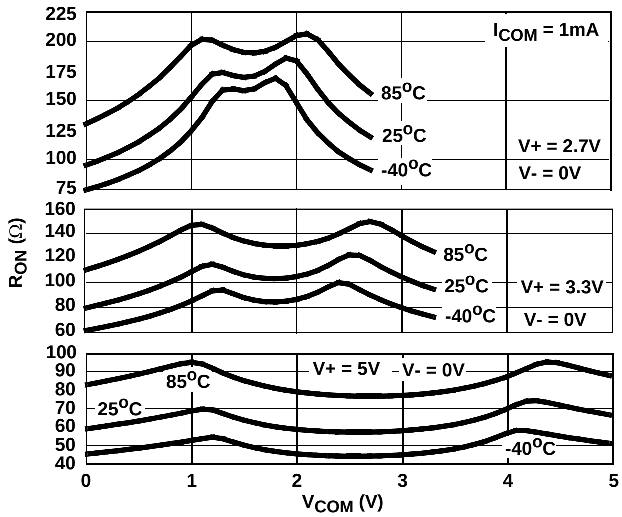


FIGURE 12. ON RESISTANCE vs SWITCH VOLTAGE

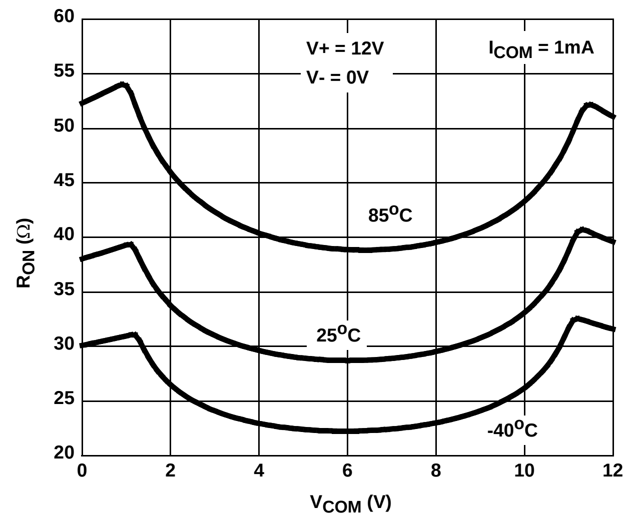


FIGURE 13. ON RESISTANCE vs SWITCH VOLTAGE

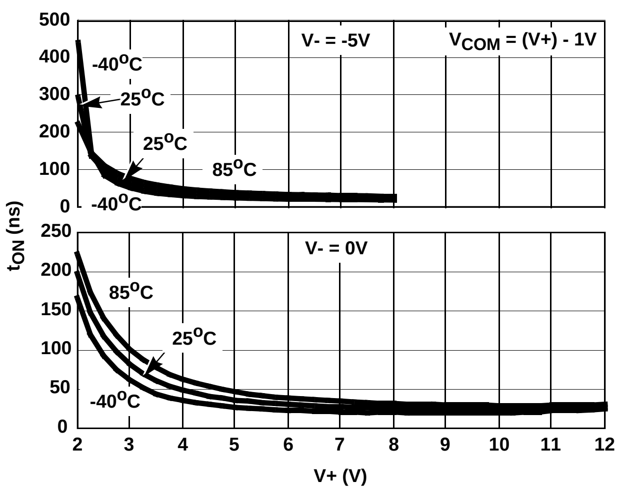


FIGURE 14. ENABLE TURN - ON TIME vs SUPPLY VOLTAGE

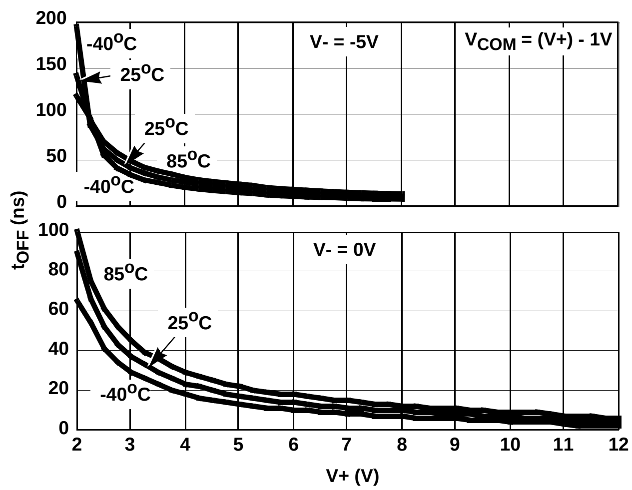


FIGURE 15. ENABLE TURN - OFF TIME vs SUPPLY VOLTAGE

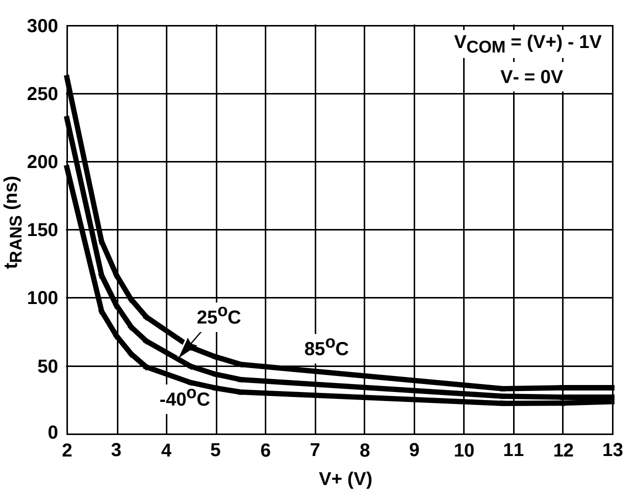


FIGURE 16. ADDRESS TRANS TIME vs SINGLE SUPPLY VOLTAGE

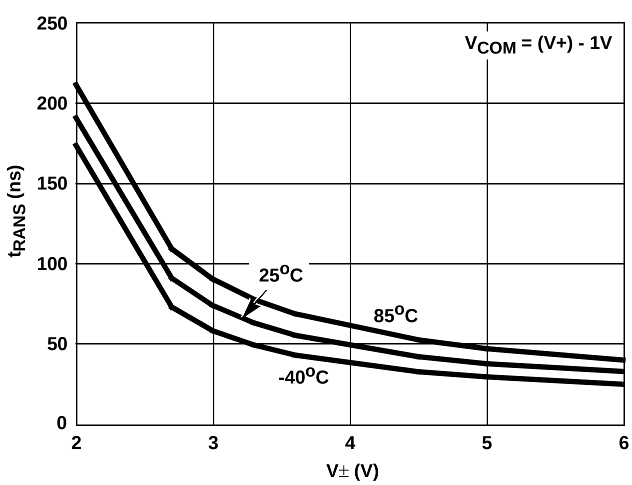


FIGURE 17. ADDRESS TRANS TIME vs DUAL SUPPLY VOLTAGE

Typical Performance Curves $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

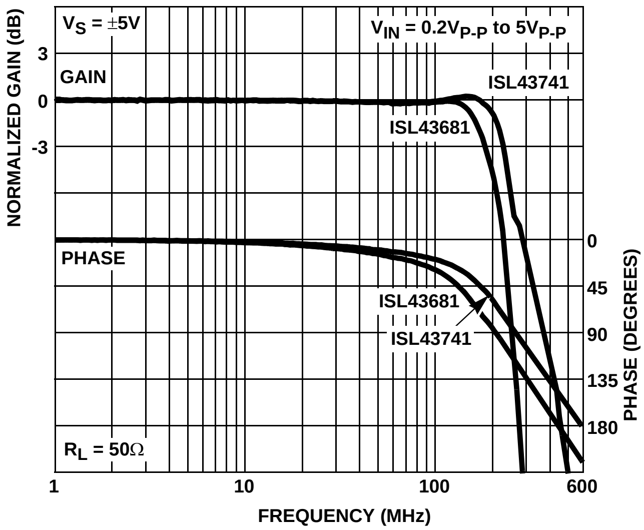


FIGURE 18. FREQUENCY RESPONSE

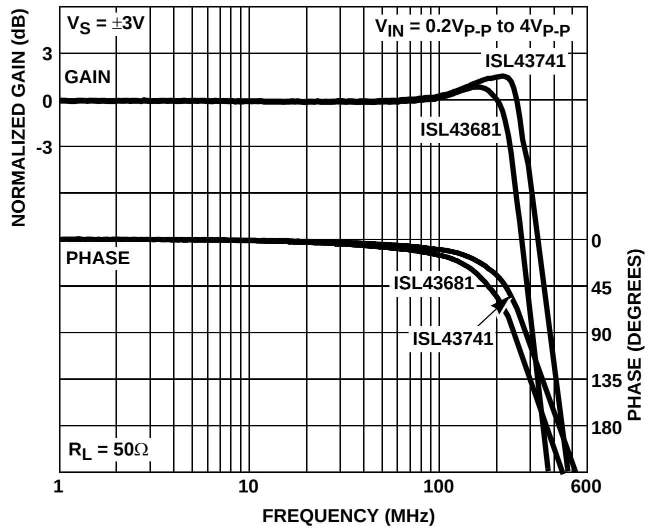


FIGURE 19. FREQUENCY RESPONSE

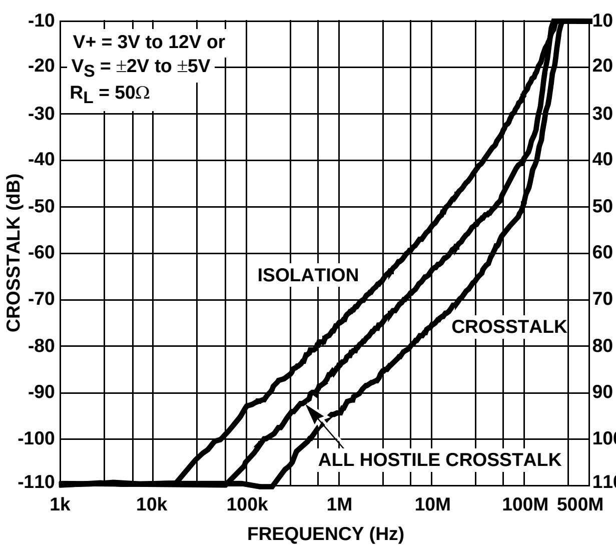


FIGURE 20. CROSSTALK AND OFF ISOLATION

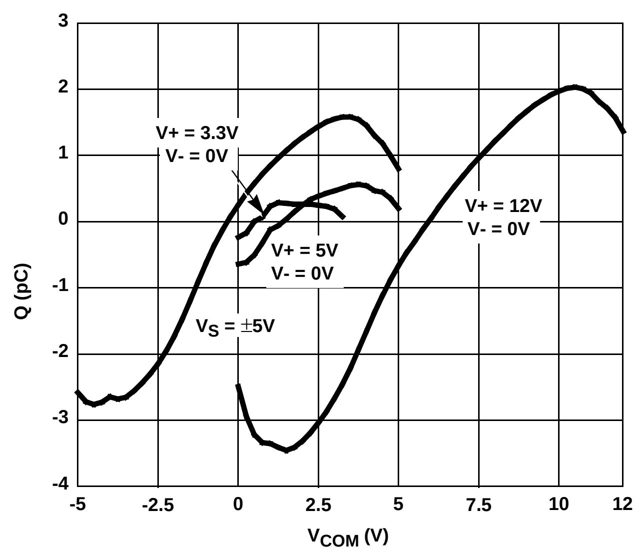


FIGURE 21. CHARGE INJECTION vs SWITCH VOLTAGE

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

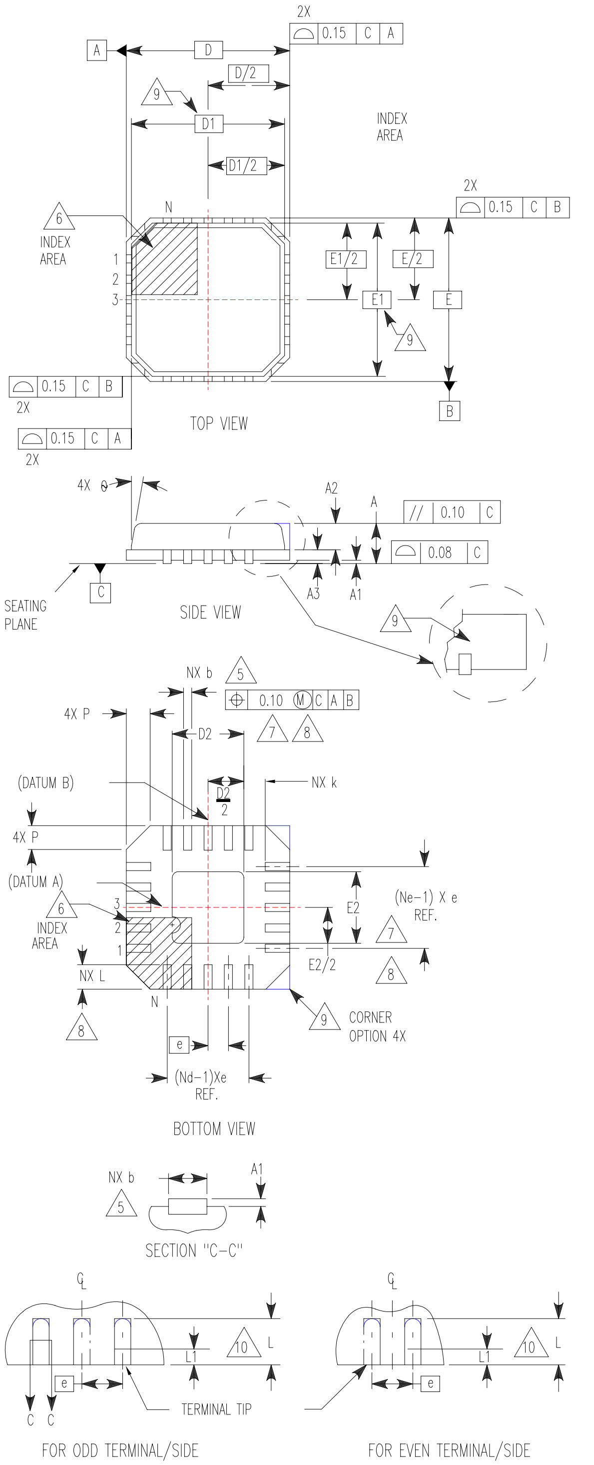
TRANSISTOR COUNT:

ISL43681: 193
ISL43741: 193

PROCESS:

Si Gate CMOS

Quad Flat No-Lead Plastic Package (QFN) Micro Lead Frame Plastic Package (MLFP)



L20.4x4

20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VGGD-1 ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.18	0.23	0.30	5, 8
D		4.00 BSC		-
D1		3.75 BSC		9
D2	1.95	2.10	2.25	7, 8
E		4.00 BSC		-
E1		3.75 BSC		9
E2	1.95	2.10	2.25	7, 8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.35	0.60	0.75	8
L1	-	-	0.15	10
N		20		2
Nd		5		3
Ne	5	5		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 1 10/02

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.